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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,765	09/10/2003	Yukiya Hirabayashi	116801	4078

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EXAMINER	
SCHECHTER, ANDREW M	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 01/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/658,765	HIRABAYASHI, YUKIYA	
	Examiner	Art Unit	
	Andrew Schechter	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/19/05, 10/31/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *IDS 11/21/05, IDS 12/29/05*.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 2 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 2 recites the limitation that the sample hold circuit of the peripheral driving circuit is disposed completely within the sealed region (as shown in Figs. 1 and 2, first embodiment) and also recites that the counter substrate is in a non-overlapping arrangement with the peripheral driving circuit (as shown in Figs. 4 and 5, second embodiment). There is no single embodiment or figure disclosing the claimed invention, for the very good reason that the limitations are mutually contradictory. The entire sealed region must be overlapped with the counter substrate, so if part of the peripheral driving circuit is within the sealed region, then the peripheral driving circuit cannot be in a non-overlapping arrangement with the counter substrate.

Claim 2 is therefore rejected.

Claim Objections

3. Claim 6 is objected to because of the following informalities: "plurality of pixel electrode" in line 3 should be "plurality of pixel electrodes". Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 and 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Sawatsubashi et al.,* U.S. Patent No. 5,148,301 in view of *Shirahashi et al.,* U.S. Patent No. 5,285,301 and further in view of *Dill et al.,* U.S. Patent No. 3,862,360.

Sawatsubashi discloses [see Figs. 3-5] an electro-optical device comprising an active matrix substrate [101] having on the same plane a plurality of scanning lines [G1-Gm], a plurality of signal lines [D1-Dn] provided to intersect the scanning lines, a plurality of pixel electrodes [103] provided at the intersection portions of the scanning and signal lines, a peripheral driving circuit [112, 113] to matrix drive the pixel electrodes, and wiring lines [114] for supplying signals to the peripheral driving circuit, the peripheral driving circuit including thin film transistors [col. 4, lines 58-62] each having a channel region [a channel region is an inherent part of a TFT, part of the semiconductor mentioned in the previous citation]; a counter substrate [102] having a

common electrode [105] facing the pixel electrodes; a seal [108] that forms a sealed region between the substrate, with the peripheral driving circuit being disposed completely within the sealed region and the wiring being disposed at least partially within the seal [see Figs. 3 and 4, and col. 4, lines 62-66]; a liquid crystal layer [109] disposed in the sealed region between the active matrix substrate and the counter substrate; wherein the common electrode is in a non-overlapping arrangement with both the peripheral driving circuit and wiring lines in plan view.

Sawatsubashi does not explicitly disclose a light shielding film on the counter substrate which is in a non-overlapping arrangement with both of the peripheral driving circuit and wiring lines. *Shirahashi* discloses [see Fig. 15, for instance] a light shielding film [BM] on the counter substrate which is in a non-overlapping arrangement with both of the peripheral driving circuit and wiring lines [the black matrix covers only the dummy pixel regions and the non-display areas of the pixels]. It would have been obvious to one of ordinary skill in the art at the time of the invention to use such a black matrix in the device of *Sawatsubashi*, motivated by the teaching of *Shirahashi* that it protects the semiconductor layers and clarifies the contour of each pixel to improve the contrast [col. 9, lines 9-45].

Sawatsubashi does not explicitly disclose that the peripheral driving circuit includes a sample hold circuit with TFTs. *Dill* discloses [see Figs. 8-10] an analogous LCD with an analogous peripheral driving circuit, which does include such a sample hold circuit. It would have been obvious to one of ordinary skill in the art at the time of the invention to use such a sample hold circuit in the device of *Sawatsubashi,* motivated

by the teaching of *Dill* that this enables a line of conventional video data to be sampled and displayed on the screen [col. 5, lines 15ff].

Claim 1 is therefore unpatentable.

Sawatsubashi's peripheral driving circuit comprises a data line driving circuit [112] (and *Dill* teaches a sample hold circuit, of course), and the wiring lines comprise clock signal lines and image signal lines [col. 5, lines 33-38], so claim 5 is also unpatentable. It is an electronic apparatus, so claim 7 is also unpatentable.

Considering claim 6: as discussed above, *Sawatsubashi* in view of *Shirahashi* in view of *Dill* discloses a method of manufacturing an electro-optical device, comprising forming a plurality of pixel electrodes [103] and a peripheral driving circuit [112, 113] to matrix drive the plurality of pixel electrodes, and wiring lines [114] for supplying signals to the peripheral driving circuit on one surface of an active matrix substrate [101], the peripheral driving circuit including a sample hold circuit with TFTs each having a channel region; forming a common electrode [105] and light shielding film on one surface of a counter substrate [102] and arranging both of them in a non-overlapping arrangement with both of the peripheral driving circuit and the wiring lines in plan view; bonding the active matrix substrate to the counter substrate with a predetermined gap using a sealing material [108] to form a sealed region, the peripheral driving circuit and its sample hold circuit being disposed completely within the sealed region and wiring being disposed at least partially within the seal, and the common electrode facing the pixel electrodes; and forming a liquid crystal layer by injecting liquid crystal into the

sealed region formed by the active matrix substrate, the counter substrate, and the sealing material [col. 4, lines 40-42]. Claim 6 is therefore unpatentable as well.

6. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Sawatsubashi* in view of *Shirahashi* in view of *Dill* as applied to claim 1 above, and further in view of *Yamamoto et al.*, U.S. Patent No. 5,506,705.

Sawatsubashi does not disclose single crystal silicon TFTs or driving signals to the peripheral driving circuit at a frequency equal to or more than 10 MHz. For an analogous LCD, *Yamamoto* discloses using single crystal silicon TFTs and a driving signal of 10 MHz [col. 12, lines 1-25]. It would have been obvious to one of ordinary skill in the art at the time of the invention to use single crystal silicon TFTs and a 10 MHz driving frequency in the device of *Sawatsubashi*, motivated by *Yamamoto's* teaching that this allows high speed driving and thus improves the display quality. Claims 3 and 4 are therefore unpatentable.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

JP 11-101985 to *Kimura*, made of record by the applicant, discloses and teaches having the peripheral driving circuitry inside the seal region and in a non-overlapping arrangement with the common electrode, and the wiring lines partially within the seal.

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Schechter whose telephone number is (571) 272-2302. The examiner can normally be reached on Monday - Friday, 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on (571) 272-2293. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Andrew Schechter
Primary Examiner
Technology Center 2800
13 January 2006